

CLAIM LISTING

1. (Original) An apparatus that uses pseudo-differential voltage
2 signaling, comprising:

3 a reference receiver that receives an undistributed reference voltage and in
4 response produces a buffered voltage that is derived at least in part from the
5 undistributed reference voltage;

6 signal receivers associated respectively with a plurality of signal voltages;

7 wherein an individual signal receiver receives both its associated signal
8 voltage and the buffered voltage, and;

9 wherein said individual signal receiver evaluates its associated signal
10 voltage and the buffered voltage to produce an output voltage.

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12 2. (Original) An apparatus as recited in claim 1, wherein said
13 individual signal receiver evaluates by comparing the associated signal voltage
14 and the buffered voltage to produce an output voltage.

15
16 3. (Original) An apparatus as recited in claim 1, wherein the buffered
17 voltage is the difference between the undistributed reference voltage and a
18 distributed reference voltage.

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20 4. (Original) An apparatus as recited in claim 1, wherein the buffered
21 voltage is proportional to the undistributed reference voltage.

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1 5. (Original) An apparatus as recited in claim 1, wherein the buffered
2 voltage represents the noise of the signal voltages relative to the undistributed
3 reference voltage.

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5 6. (Original) An apparatus as recited in claim 1, wherein the reference
6 receiver also receives a distributed reference voltage that is received by the signal
7 receivers, wherein the reference receiver is responsive to the distributed reference
8 voltage and the undistributed reference voltage to produce the buffered voltage.

9
10 7. (Original) An apparatus as recited in claim 1, wherein the reference
11 receiver also receives a distributed reference voltage that is received by the signal
12 receivers, wherein the reference receiver compares the distributed reference
13 voltage and the undistributed reference voltage to produce the buffered voltage.

14
15 8. (Original) An apparatus as recited in claim 1, wherein the reference
16 receiver also receives a distributed reference voltage that is received by the signal
17 receivers, wherein the reference receiver compares the distributed reference
18 voltage and the undistributed reference voltage to produce the buffered voltage,
19 the buffered voltage representing the difference between the distributed reference
20 voltage and the undistributed reference voltage.

21
22 9. (Original) An apparatus as recited in claim 1, further comprising:
23 a plurality of signal buffers that receive the signal voltages and in response
24 produce buffered signal voltages, wherein each buffered signal voltage is subject
25 to a signal capacitance;

1 the buffered voltage being subject to a reference capacitance that is
2 significantly greater than the signal capacitance;

3 each of the signal buffers having a first electrical current capacity;

4 the reference receiver having a second electrical current capacity that is
5 greater than the first electrical current capacity by a ratio equal to the ratio of the
6 reference capacitance to the signal capacitance.

7
8 10. (Original) An apparatus as recited in claim 1, further comprising:

9 a plurality of signal buffers that receive the signal voltages and in response
10 produce buffered signal voltages, wherein each buffered signal voltage is subject
11 to a signal capacitance;

12 the buffered voltage being subject to a reference capacitance that is
13 significantly greater than the signal capacitance;

14 each of the signal buffers having a first electrical current capacity;

15 the reference receiver having a second electrical current capacity that is
16 greater than the first electrical current capacity by a ratio equal to the ratio of the
17 reference capacitance to the signal capacitance; and

18 wherein the reference receiver and the signal buffers are source-followers.

19
20 11. (Original) An apparatus as recited in claim 1, further comprising:

21 a plurality of signal buffers that receive the signal voltages and in response
22 produce buffered signal voltages.

23
24 12. (Original) An apparatus as recited in claim 1, further comprising:

1 a plurality of signal buffers that receive the signal voltages and in response
2 produce buffered signal voltages;

3 wherein the reference receiver and the signal buffers are source-followers.

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5 13. (Original) An apparatus as recited in claim 1, wherein the reference
6 receiver has a unity gain.

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8 14. (Original) An apparatus as recited in claim 1, wherein:
9 the signal voltage has associated input capacitance and inductance that
10 result in a resonant input frequency;
11 the reference receiver has a bandwidth that is significantly greater than the
12 resonant input frequency.

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14
15 15. (Original) An apparatus as recited in claim 1, wherein:
16 the signal voltage has associated input capacitance and inductance that
17 result in a resonant input frequency;
18 the reference receiver has a bandwidth of at least ten times the resonant
19 input frequency.

20
21 16. (Original) An apparatus as recited in claim 1, wherein each signal
22 voltage represents one of two values and the signal receivers compare the buffered
23 voltage and the signal voltages to determine which of the two values is represented
24 by each signal voltage.

1 17. (Original) An apparatus as recited in claim 1, the reference voltage
2 and the buffered voltage being subject to similar impedances.

3
4 18. (Currently Amended) An apparatus as recited in claim 1, the
5 reference voltages and signal voltage being subject to similar impedances, wherein
6 coupled signal noise is introduced approximately equally in the buffered voltage
7 and the plurality of pseudo-differential signal voltages, said approximately equal
8 coupled signal noise being canceled in the evaluation performed by the signal
9 receiver.

10
11 19. (Original) An integrated circuit comprising:
12 a reference input that receives a common reference voltage;
13 a plurality of signal inputs configured to receive pseudo-differential signal
14 voltages that represent values in terms of relationships between the pseudo-
15 differential signal voltages and the common reference voltage;
16 a reference buffer that receives the common reference voltage and in
17 response produces a buffered reference voltage;
18 signal comparators associated respectively with the plurality of pseudo-
19 differential signal voltages, each signal comparator comparing the buffered
20 reference voltage and one of the pseudo-differential signal voltages to determine
21 the value represented by said one of the pseudo-differential signal voltages;
22 wherein the reference and signal inputs have similar impedances, coupled
23 signal noise being introduced approximately equally in the buffered reference
24 voltage and the plurality of pseudo-differential signal voltages, said approximately

1 equal coupled signal noise being canceled in the comparison performed by the
2 signal comparators.

3
4 20. (Original) An integrated circuit as recited in claim 19, further
5 comprising:

6 a plurality of signal buffers that receive the pseudo-differential signal
7 voltages and in response produce buffered signal voltages, wherein each buffered
8 signal voltage is subject to a signal capacitance;

9 the buffered reference voltage being subject to a reference capacitance that
10 is significantly greater than the signal capacitance;

11 each of the signal buffers having a first electrical current capacity;

12 the reference buffer having a second electrical current capacity that is
13 greater than the first electrical current capacity by a ratio equal to the ratio of the
14 reference capacitance to the signal capacitance.

15
16 21. (Original) An integrated circuit as recited in claim 19, further
17 comprising:

18 a plurality of signal buffers that receive the pseudo-differential signal
19 voltages and in response produce buffered signal voltages, wherein each buffered
20 signal voltage is subject to a signal capacitance;

21 the buffered reference voltage being subject to a reference capacitance that
22 is significantly greater than the signal capacitance;

23 each of the signal buffers having a first electrical current capacity;

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1 the reference buffer having a second electrical current capacity that is
2 greater than the first electrical current capacity by a ratio equal to the ratio of the
3 reference capacitance to the signal capacitance; and
4 wherein the reference buffer and the signal buffers are source-followers.

5
6 22. (Original) An integrated circuit as recited in claim 19, further
7 comprising:

8 a plurality of signal buffers that receive the pseudo-differential signal
9 voltages and in response produce buffered signal voltages for comparison by the
10 signal comparators.

11
12 23. (Original) An integrated circuit as recited in claim 19, further
13 comprising:

14 a plurality of signal buffers that receive the pseudo-differential signal
15 voltages and in response produce buffered signal voltages;

16 wherein the reference buffer and the signal buffers are source-followers.

17
18 24. (Original) An integrated circuit as recited in claim 19, wherein the
19 reference buffer has a unity gain.

20
21 25. (Original) An integrated circuit as recited in claim 19, wherein:

22 the signal inputs have associated input capacitances and inductances that
23 result in a resonant input frequency;

24 the reference buffer has a bandwidth that is significantly greater than the
25 resonant input frequency.

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2 26. (Original) An integrated circuit as recited in claim 19, wherein:
3 the signal input has associated input capacitance and inductance that result
4 in a resonant input frequency;

5 the reference buffer has a bandwidth of at least ten times the resonant input
6 frequency.

7
8 27. (Original) An integrated circuit as recited in claim 19, wherein each
9 signal voltage represents one of two values and the signal comparators compare
10 the buffered reference voltage and the signal voltages to determine which of the
11 two values is represented by each signal voltage.

12
13 28. (Original) An integrated circuit as recited in claim 19, the reference
14 and signal inputs having matching impedances.

15
16 29. (Original) A system comprising:
17 a first integrated circuit that transmits a common reference voltage and a
18 plurality of pseudo-differential signal voltages, wherein the pseudo-differential
19 signal voltages represent values in terms of relationships between the pseudo-
20 differential signal voltages and the common reference voltage;

21 a second integrated circuit that receives the common reference voltage and
22 the plurality of pseudo-differential signal voltages;

23 the second integrated circuit having a reference buffer that receives the
24 common reference voltage and in response produces a buffered reference voltage;

25

1 the second integrated circuit having signal comparators associated
2 respectively with the plurality of pseudo-differential signal voltages, each signal
3 comparator comparing the buffered reference voltage and a respective one of the
4 pseudo-differential signal voltages to determine the value represented by said one
5 of the pseudo-differential signal voltages;

6 wherein the second integrated circuit is configured to introduce
7 approximately equal coupled signal noise in the buffered reference voltage and the
8 plurality of pseudo-differential signal voltages, said approximately equal coupled
9 signal noise being canceled in the comparisons performed by the signal
10 comparators.

11
12 30. (Original) A system as recited in claim 29, the second integrated
13 circuit further comprising:

14 a plurality of signal buffers that receive the pseudo-differential signal
15 voltages and in response produce buffered signal voltages, wherein each buffered
16 signal voltage is subject in the second integrated circuit to a signal capacitance;

17 the buffered reference voltage being subject in the second integrated circuit
18 to a reference capacitance that is significantly greater than the signal capacitance;

19 each of the signal buffers having a first electrical current capacity;

20 the reference buffer having a second electrical current capacity that is
21 greater than the first electrical current capacity by a ratio equal to the ratio of the
22 reference capacitance to the signal capacitance.

23
24 31. (Original) A system as recited in claim 29, the second integrated
25 circuit further comprising:

1 a plurality of signal buffers that receive the pseudo-differential signal
2 voltages and in response produce buffered signal voltages, wherein each buffered
3 signal voltage is subject in the second integrated circuit to a signal capacitance;

4 the buffered reference voltage being subject in the second integrated circuit
5 to a reference capacitance that is significantly greater than the signal capacitance;

6 each of the signal buffers having a first electrical current capacity;

7 the reference buffer having a second electrical current capacity that is
8 greater than the first electrical current capacity by a ratio equal to the ratio of the
9 reference capacitance to the signal capacitance; and

10 wherein the reference buffer and the signal buffers are source-followers.

11 *PL*
12 32. (Original) A system as recited in claim 29, the second integrated
13 circuit further comprising:

14 a plurality of signal buffers that receive the pseudo-differential signal
15 voltages and in response produce buffered signal voltages.

16
17 33. (Original) A system as recited in claim 29, the second integrated
18 circuit further comprising:

19 a plurality of signal buffers that receive the pseudo-differential signal
20 voltages and in response produce buffered signal voltages;

21 wherein the reference buffer and the signal buffers are source-followers.

22
23 34. (Original) A system as recited in claim 29, wherein the reference
24 buffer is a unity gain amplifier.

1 35. (Original) A system as recited in claim 29, wherein:

2 the second integrated circuit has signal inputs that receive the plurality of
3 signal voltages, the signal inputs having associated input capacitance and
4 inductance that result in a resonant input frequency;

5 the reference buffer has a bandwidth that is significantly greater than the
6 resonant input frequency.

7
8 36. (Original) A system as recited in claim 29, wherein:

9 the second integrated circuit has signal inputs that receive the plurality of
10 signal voltages, the signal inputs having associated input capacitance and
11 inductance that result in a resonant input frequency;

12 the reference buffer has a bandwidth of at least ten times the resonant input
13 frequency.

14
15 37. (Original) A system as recited in claim 29, wherein each pseudo-
16 differential signal voltage represents one of two values and the comparators
17 compare the buffered reference voltage and the pseudo-differential signal voltages
18 to determine which of the two values is represented by each pseudo-differential
19 signal voltage.

20
21 38. (Original) A system as recited in claim 29, wherein the second
22 integrated circuit has signal inputs that receive the pseudo-differential signal
23 voltages and a reference input that receives the common reference voltage, the
24 reference and signal inputs having similar impedances.

1 39. (Original) A method comprising:

2 receiving a reference voltage;

3 receiving a plurality of signal voltages;

4 producing a buffered voltage based at least in part on the reference voltage;

5 evaluating the buffered voltage and one of the signal voltages to determine

6 a value represented by said one of the signal voltages.

7

8 40. (Original) A method as recited in claim 39, wherein the evaluating

9 comprises comparing said one of the signal voltages and the buffered voltage to

10 produce an output voltage.

11

12 41. (Original) A method as recited in claim 39, wherein the buffered

13 voltage is the difference between an undistributed reference voltage and a

14 distributed reference voltage.

15

16 42. (Original) A method as recited in claim 39, wherein the buffered

17 voltage is proportional to the reference voltage.

18

19 43. (Original) A method as recited in claim 39, wherein the buffered

20 voltage represents the noise of the signal voltages.

21

22 44. (Original) A method as recited in claim 39, said producing

23 comprising comparing a distributed reference voltage that is received by the signal

24 receivers and an undistributed reference voltage that is not received by the signal

25 receivers.

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2 45. (Original) A method as recited in claim 39, said producing
3 comprising comparing a distributed reference voltage that is received by the signal
4 receivers and a undistributed reference voltage that is not received by the signal
5 receivers, the buffered voltage representing the difference between the
6 undistributed reference voltage and the distributed reference voltage.

7
8 46. (Original) A method as recited in claim 39, further comprising:
9 buffering the signal voltages with signal buffers to produce buffered signal
10 voltages, wherein each buffered signal voltage is subject to a signal capacitance;

11 said producing the buffered voltage being performed with a reference
12 buffer, the buffered voltage being subject to a reference capacitance that is
13 significantly greater than the signal capacitance;

14 each of the signal buffers having a first electrical current capacity;
15 the reference buffer having a second electrical current capacity that is
16 greater than the first electrical current capacity by a ratio equal to the ratio of the
17 reference capacitance to the signal capacitance.

18
19 47. (Original) A method as recited in claim 39, further comprising:

20 buffering the signal voltages with source-follower signal buffers to produce
21 buffered signal voltages, wherein each buffered signal voltage is subject to a
22 signal capacitance;

23 said producing the buffered voltage being performed with a source-follower
24 reference buffer, the buffered voltage being subject to a reference capacitance that
25 is significantly greater than the signal capacitance;

1 each of the signal buffers having a first electrical current capacity;
2 the reference buffer having a second electrical current capacity that is
3 greater than the first electrical current capacity by a ratio equal to the ratio of the
4 reference capacitance to the signal capacitance.

5
6 48. (Original) A method as recited in claim 39, further comprising:
7 buffering the signal voltages to produce buffered signal voltages.

8
9 49. (Original) A method as recited in claim 39, further comprising:
10 buffering the signal voltages with source-followers to produce buffered
11 signal voltages.

12
13 50. (Original) A method as recited in claim 39, wherein:
14 the signal voltages are received by signal inputs having associated input
15 capacitances and inductances that define a resonant frequency;
16 producing the buffered voltage with a unity gain buffer having a bandwidth
17 that is significantly greater than the resonant frequency.

18
19 51. (Original) A method as recited in claim 39, wherein:
20 the signal voltages are received by signal inputs having associated input
21 capacitances and inductances that define a resonant input frequency;
22 producing the buffered voltage with a unity gain buffer having a bandwidth
23 of at least ten times the resonant input frequency.

24
25 52. (Original) A method as recited in claim 39, wherein:

1 the reference voltage is received by a reference input;
2 the signal voltages are received by signal inputs; and
3 the reference and signal inputs have similar impedances.

4

5 53. (Original) A method as recited in claim 39, further comprising
6 introducing coupled signal noise approximately equally in the buffered reference
7 voltage and the plurality of signal voltages, said approximately equal coupled
8 signal noise being canceled in the comparing.

9

10 54. (Original) An apparatus that uses pseudo-differential voltage
11 signaling, comprising:

12 signal receivers associated respectively with a plurality of signal voltages;
13 a reference receiver that receives both an undistributed reference voltage
14 and a distributed reference voltage, wherein the distributed reference voltage is
15 distributed to the signal receivers and the undistributed reference voltage is not
16 distributed to the signal receivers;

17 wherein the reference receiver evaluates the undistributed reference voltage
18 and the distributed reference voltage to produce a buffered voltage that represents
19 the difference between the undistributed reference voltage and the distributed
20 reference voltage;

21 wherein an individual signal receiver receives both its associated signal
22 voltage and the buffered voltage; and

23 wherein said individual signal receiver adjusts its associated signal voltage
24 by the buffered voltage to produce an output voltage.

1 55. (Original) An apparatus as recited in claim 54, wherein said signal
2 receivers are two-stage receivers.

3
4 56. (Original) An apparatus as recited in claim 54, wherein said signal
5 receivers are two-stage receivers, the second stage of the receivers adjusting the
6 signal voltages.

7
8 57. (Original) An apparatus as recited in claim 54, wherein the buffered
9 voltage represents the noise of the signal voltages relative to the undistributed
10 reference voltage.

11
12 58. (Original) An apparatus as recited in claim 54, wherein the buffered
13 voltage is a differential voltage.

14
15 59. (Original) An integrated circuit that uses pseudo-differential voltage
16 signaling, comprising:

17 two-stage receivers associated respectively with a plurality of signal
18 voltages;

19 a reference receiver that receives both an undistributed reference voltage
20 and a distributed reference voltage, wherein the distributed reference voltage is
21 distributed to the signal receivers and the undistributed reference voltage is not
22 distributed to the signal receivers;

23 wherein the reference receiver compares the undistributed reference voltage
24 and the distributed reference voltage to produce a buffered voltage that represents

25

1 the difference between the undistributed reference voltage and the distributed
2 reference voltage;

3 wherein the first stage of an individual signal receiver compares its
4 associated signal voltage to the distributed reference voltage to produce a voltage
5 differential signal; and

6 wherein the second stage of said individual two-stage receiver adjusts the
7 voltage differential signal by the buffered voltage to produce an output voltage.

8
9 60. (Original) An apparatus as recited in claim 59, the two-stage receiver
10 has an input impedance similar to that of the reference receiver.

11
12 61. (Original) An apparatus as recited in claim 59, wherein the buffered
13 voltage represents the noise of the signal voltages relative to the undistributed
14 reference voltage.

15
16 62. (Original) An apparatus as recited in claim 59, wherein the buffered
17 voltage is a differential voltage.

18
19 63. (Original) A system comprising:

20 a first integrated circuit that transmits a common reference voltage and a
21 plurality of pseudo-differential signal voltages, wherein the pseudo-differential
22 signal voltages represent values in terms of relationships between the pseudo-
23 differential signal voltages and the common reference voltage;

24 a second integrated circuit that receives the common reference voltage and
25 the plurality of pseudo-differential signal voltages;

1 the second integrated circuit having a reference receiver that receives the
2 common reference voltage and in response produces a buffered voltage;

3 the second integrated circuit having two-stage signal receivers associated
4 respectively with the plurality of pseudo-differential signal voltages, each two-
5 stage signal receiver adjusting one of the pseudo-differential signal voltages by the
6 buffered voltage to produce an output voltage.

7
8 64. (Original) A system as recited in claim 63, wherein each two-stage
9 signal receiver has an input impedance similar to that of the reference receiver.

10
11 65. (Original) A system as recited in claim 63, wherein:
12 the reference receiver compares a distributed common reference voltage to
13 an undistributed common reference voltage to produce the buffered voltage;

14 the first stage of an individual two-stage signal receiver compares its
15 associated pseudo-differential signal voltage to a distributed reference voltage to
16 produce a voltage differential signal; and

17 the second stage of said individual two-stage signal receiver adjusts the
18 voltage differential signal by the buffered voltage to produce an output voltage.

19
20 66. (Original) A system as recited in claim 63, wherein the buffered
21 voltage represents the noise of the signal voltages.

22
23 67. (Original) A system as recited in claim 63, wherein the buffered
24 voltage is a differential voltage.